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Novel 8-3 encoder using single electron tunneling technology

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Abstract

Single Electron Tunneling (SET) technology introduces more potential for feature size decrease compared to well-established silicon-based CMOS technology. The SET technology offers the ability to control the motion of individual electrons in the designed circuits. In this paper, we present a single-electron 8-3 encoder built using single-electron devices. The circuit is designed using a proper tool based on a Monte Carlo technique. The complete schematic diagrams of these basic SEC along with the corresponding simulation results (using SIMON 2.0) of these SEC are included. First a single-electron OR gate is studied and then a Novel 8-3 Encoder SET, with detailed schematic and simulation results, is presented. The results proved that the circuit was an 8-3 encoder, while the behavior of the free energy of the system (which was calculated to be 4.90x10-1 eV) and the stability diagram verified the correct functioning of the circuit.

Keywords: Coulomb blockade; electron states; single-electron tunneling; single-electron devices; encoding.
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1. Introduction

Single-electron tunneling (SET) devices exploits effects that arise due to the quantized nature of charge. Therefore, single-electron technology deals with the control of transport and position of a single or a small number of electrons. The fundamental physical principles of single electronics are the tunneling effect and the Coulomb blockade, which has been observed and studied by Gorter [1]. The small size and the low power dissipation [2, 3] of SET circuits make them useful for logic and memory circuits. Several single-electron circuits have been recently proposed in the literature: Novel XOR Gate [4], single electron 2–4 decoder [5, 10], Control–Control-Not gate [6], analog to digital converter [7], Single Electron 2-Bit Multiplier [8] and Low-Power and High-Performance 1-Bit Set Full-Adder [9]. The need for computer-aided design and simulation of single-electron circuits has long been recognized. Several simulators and simulation methods have been developed to support single-electron circuit design. SIMON is such a simulator developed by Wasshuber et al. [11].

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2. Single-electron Tunneling (SET)

Single-electron tunneling (SET) devices can monitor and manipulate the motion of individual electrons. These devices lie at the intersection of two major research trends: mesoscopic physics and the miniaturization of electronic circuits. Much of the original motivation for the studying of SET devices came from mesoscopic physics. Mesoscopic physics is a study of artificially constructed systems that exhibit quantum behavior. The systems that are fabricated are called artificial atoms because the devices that are produced behave mostly like atoms. Another important research trend that has focused attention on SET devices is the miniaturization of electronic circuits. The information technologies that are becoming increasingly important in our society are advancing rapidly to achieve the goal to manufacture cheaper circuits. The power dissipated by a circuit is one of the factors limiting the miniaturization of electronic circuits. These circuits can be made very small and dissipate little power making them potentially useful for dense integrated circuits. The Coulomb energy in these systems can be characterized by a capacitance which depends on the size of the dot and also may lie in the range of 10^{-15} F or less [11-13].

Fig. 1: (a) an overlap junction with an oxide layer (b) schematic diagram for a tunnel junction.

2.1 Coulomb Blockade

The basic concept of single-electronics is the Coulomb blockade. Consider an electroneutral small conductor, which is called an island. The island has exactly as many electrons as it has protons in its crystal lattice. The electroneutral island does not generate any appreciable electric field beyond its borders and a weak external force can bring an additional electron from outside into the island [3].

Now the net charge, Q of the island is 2e; where **e** is the elementary charge. The energy Ec required to charge an island with an electron is called Coulomb energy and is given by:

$$E_c = {e^2}/{2C_i} \quad (1)$$

Where, C_i is the capacitance of the island. Although the extra charge –e in the island is very small, the electric field generated by this charge is inversely proportional to the square of the island size and may become very strong in nanoscale structures. This strong electric field inhibits further electron transfer into the island, thus giving rise to the Coulomb blockade effect. Single- electronics exploit Coulomb blockade by representing bits of information by the presence or absence of a single-electron or a small number of electrons in conducting islands.

2.2 Monte Carlo Technique

There are currently two simulation approaches used for SET circuits. One is based on a Monte Carlo method and the other on a master equation. The Monte Carlo approach starts with all possible tunnel events, calculates their probabilities, and chooses one of the possible events randomly, weighted according to their probabilities. This is done many times to simulate the transport of electrons through the network. Tunnel events are considered to be independent and exponentially distributed. The Mote Carlo approach gives better transient and dynamic characteristics of SET circuits because it models the underlying microscopic physics in a very direct manner. In real SET circuits, electrons tunnel from island to island, as simulated by the Monte Carlo method. Tunnel events can be modeled as discrete events as long as the electrons are confined on quantum dots.

3. Device and Circuit Design

3.1 Two-input SET OR Gate

The single-electron OR gate is shown in Fig. 2. The circuit comprises three islands N1-N3 and one tunnel junctions J. The resistance and capacitance of tunnel junction value is $1x10^{5}$ Ω and $1x10^{-19}$ F respectively. A and B are the inputs to the OR gate. A and B can take only two values, 0V which corresponds to the logic '0' and 16mV which corresponds to the logic '1'. The both input voltages are applied to node N3 through the capacitors C1 and C2. Which are identical and their capacitance is $5x10^{-19}$ F. The gate output is also taken from island N3. The presence of positive charge in the output islands corresponds to logic 1, whereas no charge corresponds to logic 0. The voltage source V_{dd} is constant and its value is 16mV.

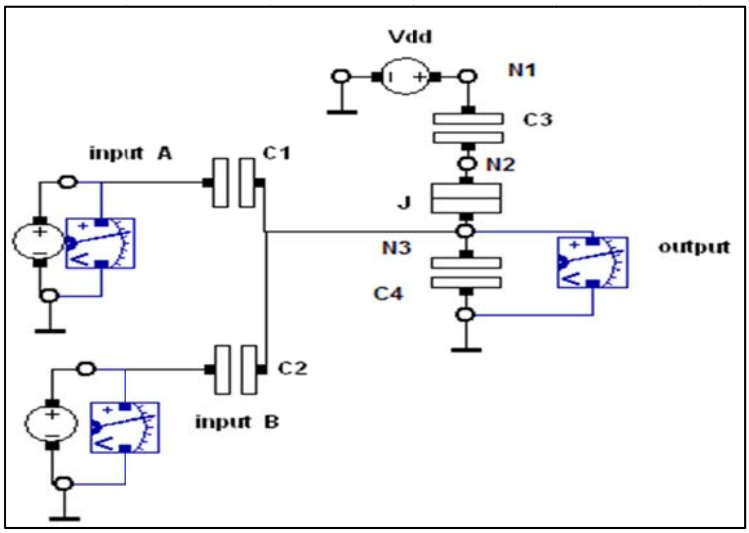

Fig. 2: Single electron OR gate.

The operation of the OR gate is shown in Fig. 3. Fig. 3(a) and (b) shows the time variation of input voltages A and B, respectively. The inputs are piece-wise constant and apply all possible combinations of logic '0' and '1' to the gate. Fig. 3(c) shows the time variation of the voltage at the output node N3. The voltage at N3 is about 16mV when the

input vectors [0 1] and [1 1] are applied to the gate. When the input vector [0 0] is applied an excess electron is transported via tunneling to island N3 and the island voltage becomes 0.0V. When the input vector [1 0] is applied, the electron tunnels out of N3 and the charge at this island becomes 16mV again.

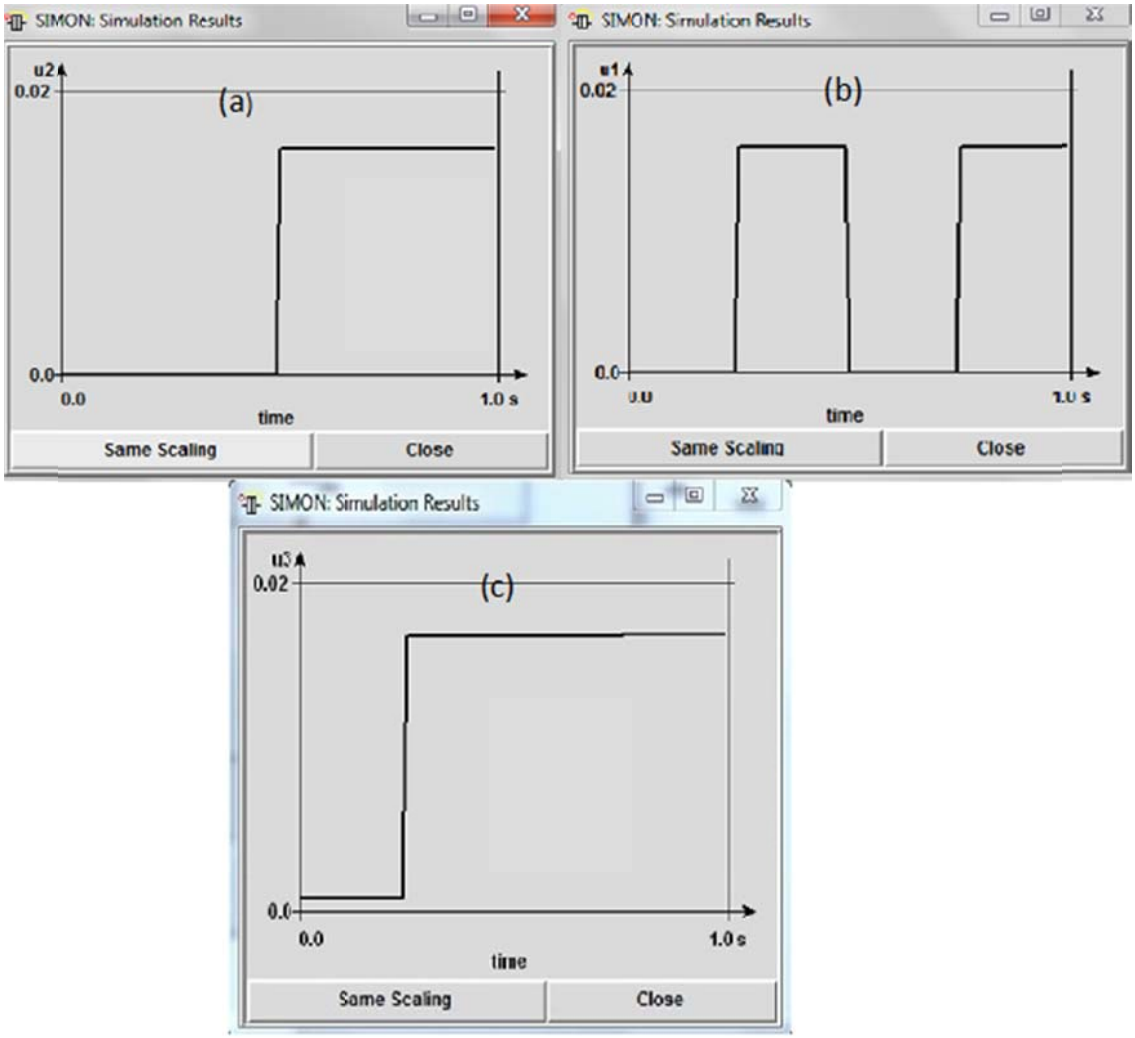

Fig. 3: Operation of the single-electron OR gate (a)Time variation of the input voltage V1; (b) time variation of the input voltage V2 and (c) time variation of the output voltage V3.

3.2 Design of the SET 8-3 Encoder

The designed single electron 8-3 encoder circuit using SIMON 2.0 is shown in Fig. 4. Hence, 9 SET OR gates are used. The circuit comprises 19 islands N1 to N19, bounded by nine tunnel junctions J1 to J9. The capacitance and their resistances value of each junction shown in Table 1. The circuit also comprises 36 capacitors, and the values are shown on Table 2. The voltage V_{dd} is constant and its value is 16mV. The input voltages are applied to node N2, N5, N9, N12, N19 through the capacitors C19, C20, C21,C22, C26, C27, C28, C31, C32, C34, C25 and C33. The input voltage Vin1 to Vin7, shown in Figure 4, are the inputs of the 8-3 encoder, named I_1 to I_7, and it can take only two values 0.0V which corresponds to the logic ‘‘0’’ and 16mV which corresponds to the logic ‘‘1’’. The output signals of the encoder are taken from islands N8, N15, and N18, named OUTPUT A, OUTPUT B and OUTPUT C respectively.

Table 1: Resistances and capacitances of tunnel junctions of the single-electron

Tunnel junction	Resistance (Ω)	Capacitance(F)
J1 –J9	$1x10^{5}$	$1x10^{-19}$
C1 – C9		$1.17x10^{-17}$
C10 – C18		$9x10^{-18}$
C19-C36		$5x10^{-19}$

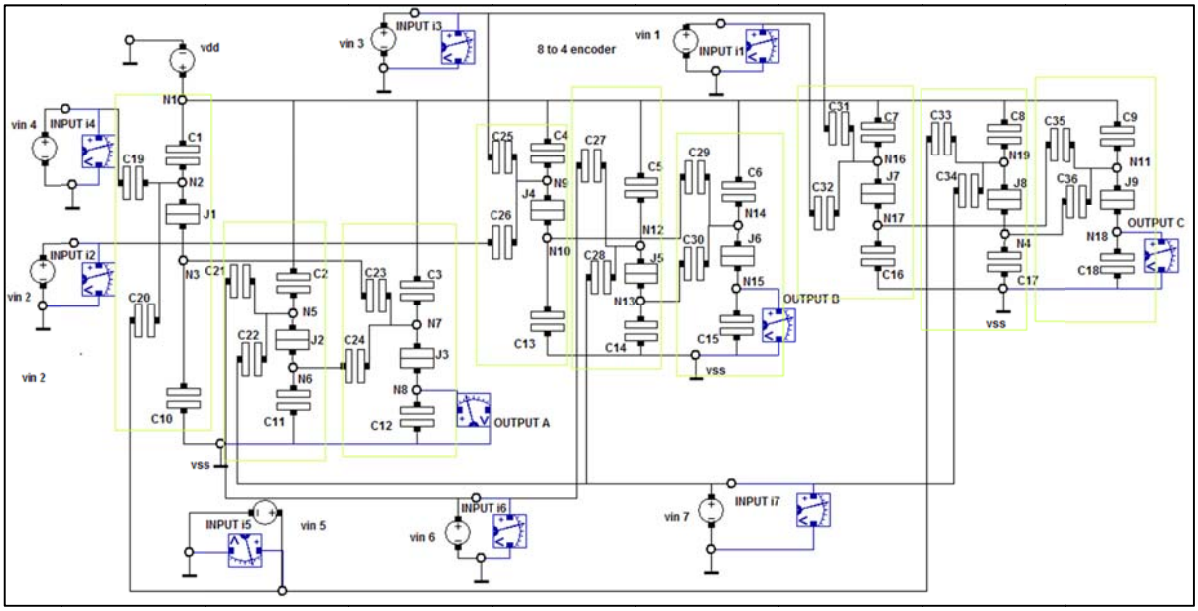

Fig. 4: Novel 8-3 single electron encoder.

This encoder OR gate circuit is at direct comparison with a similar one reported in the literature [14], which was constructed by a different tool and under a full custom design approach. This comparison raised some interesting results, which among others included that the circuit in [14] allowed less delay time, while the circuit presented here showed a substantial power consumption reduction. The Comparison between the circuit presented and analysed in Ref. [14] is shown in Table 3.

Table 3: Comparison between the circuit presented and analyzed in Ref. [14]

Circuit elements	Circuit in Ref. [20]	Circuit in this paper
Junctions	5	1
Capacitors	2	4
Islands	4	3
Voltage for logic 0 (V)	0V	0V
Voltage for logic 1(V)	0.20V	16mV
Vdd	0.22V	16mV

4. Analysis of the Encoder and Results

The 8-3 encoder needs to be analyzed the operational characteristics. From the corresponding output islands we take the outputs A, B and C, respectively. The presence of positive voltage in the output islands corresponds to logic 1, whereas no voltage corresponds to logic 0. Hence, the input–output signals, of this encoder are shown in Figure 5. The eight inputs in the circuit are encoded to three outputs, where each output symbolizes one of the minterms of the eight inputs. In this circuit we used nine single-electron OR gates to analysis the 8-3 single-electron encoder. When the input vector [10000000] is applied an excess electron is transported via tunneling to island N8, N15, N18 and the island voltage (OUTPUT A, B, C) becomes 0.0V. When the input vector is varied, the electron tunnels out of N8, N15 and N18 are charged according to the Table 4 given below.

Table 4: The corresponding points for the stability plot of the 8-3 encoder

I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	Input vector	Output vector
16mV	0V	0V	0V	0V	0V	0V	0V	10000000	000
0V	16mV	0V	0V	0V	0V	0V	0V	01000000	001
0V	0V	16mV	0V	0V	0V	0V	0V	00100000	010
0V	0V	0V	16mV	0V	0V	0V	0V	00010000	011
0V	0V	0V	0V	16mV	0V	0V	0V	00001000	100
0V	0V	0V	0V	0V	16mV	0V	0V	00000100	101
0V	0V	0V	0V	0V	0V	16mV	0V	00000010	110
0V	0V	0V	0V	0V	0V	0V	16mV	00000001	111

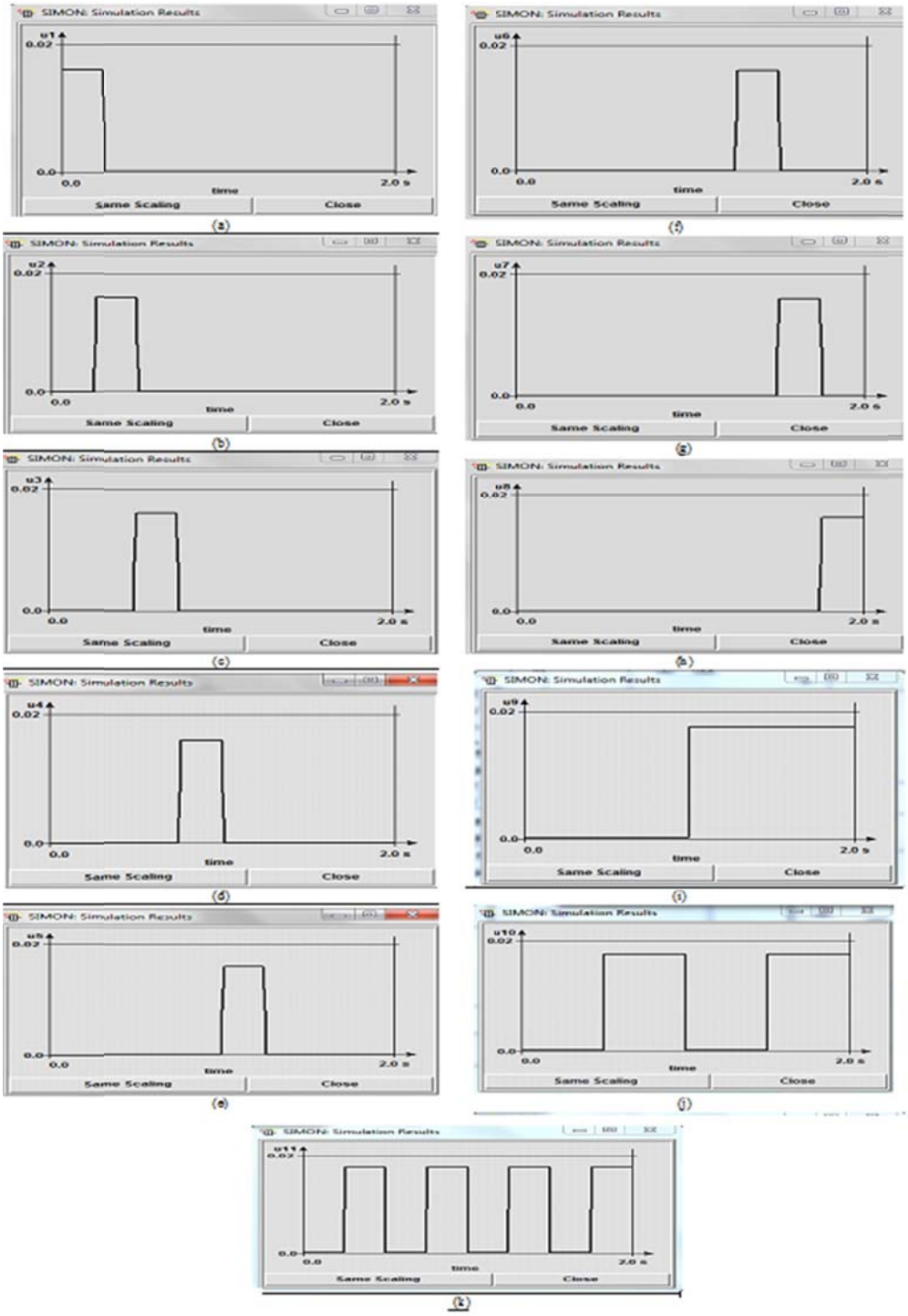

Fig. 5: Operation of the novel 8-3 single-electron encoder (a) Time variation of the input voltage V1; (b) time variation of the input voltage V2 (c) Time variation of the input voltage V3; (d) Time variation of the input voltage V4; (e)Time variation of the input voltage V5; (**f**) time variation of the input voltage V6; (g) Time variation of the input voltage V7; (h) Time variation of the input voltage V8; (i) Time variation of the output voltage A (j)time variation of the output voltage B; and (k) time variation of the output voltage C.

5. Conclusions

A single-electron 8-3 encoder was presented in this paper. A step-wise procedure was followed, designing first the OR gate, exploring its operational characteristics and knowing the individual elements operational characteristics, a 8-3 encoder circuit was built and explored using a bottom-up approach. The whole procedure was done using a Monte Carlo-based tool and the results showed a compatibility of the operating characteristics between the circuit and the individual OR gates. This outcome allows the operational characteristics of the individual gates to define those of the circuit. In all stages of the design and the simulation procedure and the operational characteristics were verified. The circuit allowed less delay time and power consumption reduction.

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